## ABSTRACT OF THE DISCLOSURE

A semiconductor device analyzer has a substrate model reading module, a Y-matrix entry module, a discriminating module, a matrix reduction module, and an output format discriminating module. The substrate model reading module reads a substrate network model of three-dimensional meshes representing the substrate of a semiconductor device. The substrate network model is a network of resistive and capacitive elements and is used for the simulation and analysis of the semiconductor substrate. The Y-matrix entry module prepares a Y-matrix from the substrate network model, each element of the Y-matrix being expressed with a polynomial of differential operator "s". The discriminating module discriminates internal nodes to be eliminated from external nodes to be left among the nodes of the substrate network model. The matrix reduction module eliminates the internal nodes, thereby reducing the Y-matrix. The output format determining module determines an output format for an operation result.